

Notice of References Cited	Application/Control No. 09/942,166	Applicant(s)/Patent Under Reexamination BLAAUW ET AL.	
	Examiner Russell L. Guill	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,946,475	08-1999	Burks et al.	716/6
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Bryant, Randal E.; McDonald, Clayton B.; "CMOS Circuit Verification With Symbolic Switch-Level Timing Simulation", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 20, Number 3, March 2001
	V	Parashkevov, Atanas Nikolaev; European Patent Application EP 1 083 500 A2
	W	Desai, Madhev P.; Yen, Y.T.; "A systematic technique for verifying critical paths delays in a 300MHz Alpha CPU design using circuit simulation", 1996, 33rd Design Automation Conference
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.